IN THE SPECIFICATION:

Page 4, last paragraph

Sub B17

In the illustrated embodiment, this bit stream is over- sampled by an eight times oversampler 17. Although an eight times over-sampler circuit is shown, any modulus of over-sampler, *e.g.*, 5, can be used without departing from the spirit and scope of the present invention. More generally, what occurs is that data transmitted at a first frequency is over-sampled using an effective clock at a second frequency, n times the receiver clock. In the example, n is eight but could also be some other number. This produces nominally [[in]] n samples per bit time (also referred to as a unit interval).

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Page 5, last paragraph:

The output from the sample word register to 19, which, in the example shown, comprises 40 samples, is applied to an edge detector 21. Edge detector 21 looks at pairs of these inputs utilizing exclusive or (XOR) gates and thereby determines that which points transitions take place. These outputs of the XOR gates are illustrated as 24a-24c of Fig. 2. The outputs of the edge detector are inputs to edge accumulation latches 23. The outputs of the edge detector will indicate, for five sets of samples at a time, between which of the eight samples a transition took place. Corresponding sample positions in each of the five sets are combined and the results latched. To get a running history, a number of latches are utilized. The edge accumulation ~~latches~~ registers 23 also receive an input from a packet state machine 20 which in turn receives an input from a squelch detector 27 having as its input the incoming signal line 13.

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Page 6, second paragraph:

The output of the edge accumulation latches is provided as an input to phase selection logic 29. In a manner to be described below, in the illustrative embodiment, the phase selection logic 29 selects, as the desired phase, the phase that is the greatest distance from the transitions. In other words, it is desired to select a phase for sampling data that is as close to the middle of the bit time as possible. The determined phase is output to the data selection register which uses it to select the data sample at that phase

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for each bit. The data selection register obtains the data from the sample word register 19.

Page 6, last paragraph:

Fig. 3 is a diagram of an embodiment of an over-sampler 17 which may be used in embodiments of the present invention. Serial data on line 51 is input to the data input of, for example, D-type flip flops 53a through 53h. Each of these is clocked by a clock signal from the clock generator 11 of Fig. 1 at the bit frequency. However, each is at a different phase. Thus, for example, flip flop 53a is clocked at zero phase, 53b at a phase of 45 degrees, 53c at a phase of 90 degrees, and so on, each phase being shifted 45 degrees from the adjacent phase. These clock phases are shown as 54a (0 deg.), 54b (45 deg.) and 54h (315 deg.) on Fig. 2. In-between clock 54b and clock 54h are additional ~~clock~~ clocks for the intervening phases. The lines 18 of Fig. 2 correspond to the leading edges of these eight clock signals.

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Page 7, last paragraph

Fig. 4 is a diagram of an exemplary embodiment of sample word register 19 of Fig. 1. The input to this unit comprises the eight lines output by the over-sampler 17. These eight lines are coupled as inputs to each of four byte registers 61a-61d. The clock generator 11 of Fig.1, in addition to generating the eight phases at the data rate, for example, 480MHz, also generates 4 clocks at 120MHz. These are shown as 62a-62d in Fig. 2. Although at the same frequency, these clocks are delayed by different amounts. The first clock 62a has no delay, the second 62b, a delay of 90 degrees, the third 62c, a delay of 180 degrees and the fourth 62d, a delay of 270 degrees. As can be seen from Fig. 2, this results in clock edges which effectively, when taken as a group, occur at a 480MHz rate. Thus, after the data has been latched into the eight latches 55a-55h of Fig. 3, which data appears on line 63, a 120MHz clock 62a transition will clock that data into byte register 61a. Then, eight more samples of data are obtained for the next data bit. This signal on line 63 is then clocked into byte register 61b by the 120MHz clock 62b delayed by 90 degrees. Similarly, the next two sets of samples are clocked into byte registers 61c and 61d by clock 62c and 62d. The output of byte register 61d is provided

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as an input to a byte register 61e. This byte register is also clocked by the 120MHz clock at zero phase. As a result, when the data is clocked into byte register 61a, at the same time, the data which had previously been stored into byte register 61d is clocked into byte register 61e. Subsequently, the data at the output of byte registers 61a-61e is clocked into a set of byte registers 65a-65e.

Page 10, first paragraph:

Thus, the latches are reset on rolling basis, under control of the packet state machine 25. For example if latch 85a is reset, it will then begin to accumulate only the most recent information. If, in succession, latch 85b, then 85c and then 85d are reset, latch [[85e]] 85d will have the oldest information 85a next oldest and so on. Thus, a rolling history of edge transitions is maintained. The outputs of the latches, of which there will be eight for each of latches ~~85a-85e~~ 85a-85d, are provided into a set of 8 OR gates 87a-87h. These OR gates then provide a historical indication of edge transitions.